IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Claire RICHTARCH	Confirmation No.: 6886
Patent No.: 7,060,620 B2	Application No.: 10/671,812
Patent Date: June 13, 2006	Filing Date: September 25, 2003
For: METHOD OF PREPARING A SURFACE OF A SEMICONDUCTOR WAFER TO MAKE IT EPIREADY	Attorney Docket No.: 4717-11300

REQUEST FOR CERTIFICATE OF CORRECTION
UNDER 37 C.F.R. §§ 1.322 and 1.323

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

Column 6:

Line 12 (claim 4, line 1), after "The method of claim **1**" insert -- wherein --.

Line 51 (claim 18, line 5), after "polishing the conditioned SiC" delete "surthee" and insert -- surface --.

Line 53 (claim 18, line 7), after "provide a wafer surface" delete "tax" and insert -- that --.

The requested changes are to correct errors of a clerical or typographical nature and do not involve changes that would constitute new matter or require reexamination.

A fee of $100 is believed to be due for this request. Please charge the required fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

6-22-06
Date

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212-294-3311

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,060,620 B2
DATED: June 13, 2006
INVENTORS: Richtarch

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6:
Line 12, after "The method of claim 1" insert -- wherein --.
Line 51, after "polishing the conditioned SiC" delete "surthee" and insert -- surface --.
Line 53, after "provide a wafer surface" delete "tax" and insert -- that --.

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Column IV shows the nature of the pad and the abrasive mixture.

Column V shows roughness measurements over a surface area of 5 micrometers (μm)×5 μm.

Comments are shown in column VI.

Table I shows that the combination of an annealing step followed by polishing can substantially reduce the roughness of the initial film to less than 2 nm rms (see tests 3–5 and 7–11), 1.5 nm (see tests 3–5 and 8–11), 1 nm rms (tests 3 and 8–11), 0.5 nm rms (tests 8–11), or 0.1 nm rms (test 11). Thus, the invention can produce a silicon carbide film with a roughness of less than 2 nm rms, less than 1 nm rms, less than 0.5 nm rms, or less than 0.1 nm rms. Use of prior ion etching, as in test number 3, also improves the result.

The best results appear to be obtained with an IC1000 pad and with a Syton W30 abrasive solution.

Table II below shows more detailed conditions concerning test numbers 10 and 11. In particular, test number 10 was carried out using an "S107" plate while test number 11 was carried out using an "S126" plate, and Table II compares roughness values using the S126 and S107 plates.

Two types of measurements were carried out: scanning a certain surface area (column S, surface area indicated in square micrometers (μm^2)), and point measurements (column B, surface measurements indicated in μm×μm).

The last three columns show, in angstroms: roughness as a root mean square value (rms), mean roughness (Ra), and maximum roughness (Rmax)

The values shown in Table I for tests 10 and 11 respectively correspond to those shown in the third and seventh lines of Table II (rms column).

TABLE II

Comparison of roughness using plates S126 and S107

Plate	S (μm^2)	B μm	rms (Å)	Ra (Å)	Rmax (Å)
S107	1 μm × 1 μm		0.97	0.77	14.7
		0.3 × 0.9	0.7	0.55	8.2
	5 μm × 5 μm		1.55	1.21	16.1
		3 × 1	1.38	1.06	12.1
S126	1 μm × 1 μm		0.37	0.28	7
		0.6 × 0.7	0.34	0.27	3
	5 μm × 5 μm		0.64	0.5	29.7
		1.5 × 4	0.31	0.25	4.9

The results shown in these tables indicate that the method according to the invention can produce a surface that is ready for epitaxy ("epiready") on thin SiC films, using a rapid technique, which employs steps and machines that are standard in microelectronics. The smoother the SiC surface and the lower its roughness, the better the quality of the epitaxy, which can substantially increase the yield of electronic components produced on the thin film. The surface preparation method of the invention, comprising an annealing step followed by polishing, can thus produce a good quality surface that is not rough and is smooth.

The example of a polytype 4H SiC substrate has been used herein, but it should be noted that the invention is also preferred for us with other SiC substrates, such as a polytype 6H substrate or to a 3C SiC substrate.

What is claimed is:

1. A method of preparing a SiC surface of a semiconductor wafer to make it epiready which comprises:
annealing the wafer in an oxidizing atmosphere to condition the SiC surface;
treating the wafer surface to reduce surface roughness; and
polishing the treated and conditioned SiC surface of the wafer with an abrasive based on particles of colloidal silica in order to provide a wafer surface that is suitable for growing an epitaxial layer thereon;
wherein the wafer is annealed under conditions sufficient to produce a surface roughness that is on the order of about 2 nm rms and the polishing step is conducted to achieve a surface roughness that is on the order of about 3 Å rms.

2. The method of claim 1 wherein the SiC surface layer is bonded to a semiconductor substrate.

3. The method of claim 1 wherein the annealing is conducted at a temperature of about 1000° C. to about 1300° C.

4. The method of claim 1, the wafer surface is treated by a deoxidizing step or by applying an RCA (SC1, SC2) type chemical cleaning step prior to polishing.

5. The method of claim 4 wherein the wafer surface is deoxidized with hydrofluoric acid.

6. The method of claim 1 wherein the treating step comprises chemically cleaning the wafer surface.

7. The method of claim 6 wherein the wafer surface is cleaned with hydrofluoric acid.

8. The method of claim 1 wherein the colloidal silica particles used for polishing the wafer surface include SYTON W30 type colloidal silica.

9. The method of claim 1 wherein the polishing is conducted with a polishing head that is rotated at about 10 rpm to about 100 rpm.

10. The method of the claim 9 which further comprises applying a pressure of about 0.1 bar to about 1 bar to the polishing head during rotation.

11. The method of claim 1 which further comprises polishing the wafer surface for about 15 minutes to about 30 minutes.

12. The method claim 1 wherein the polishing is conducted with an IC1000 type polishing pad.

13. The method of claim 1 wherein the polishing is conducted to make the wafer surface suitable for homoepitaxy or heteroepitaxy.

14. The method of claim 1 wherein the polishing is conducted to provide a surface roughness of less than 15 angstroms RMS.

15. The method of claim 1 which further comprises depositing an epitaxial layer upon the polished wafer surface.

16. The method of claim 15 wherein the epitaxial layer comprises at least one of SiC, AlN, GaN, or AlGaN.

17. The method of claim 1 wherein the conditioned surface is treated to prevent crystallization of abrasive during the polishing step.

18. A method of preparing a SiC surface of a semiconductor wafer to make it epiready which comprises:
annealing the wafer in an oxidizing atmosphere to condition the SiC surface; and
polishing the conditioned SiC surthee of the wafer with an abrasive based on particles of colloidal silica in order to provide a wafer surface tax is suitable for growing an epitaxial layer thereon,
wherein the annealing is conducted for about 1 hour to about 3 hours.

19. A method of preparing a SiC surface of a semiconductor wafer to make it epiready which comprises:
annealing the wafer in an oxidizing atmosphere to condition the SiC surface;
polishing the conditioned SiC surface of the wafer with an abrasive based on particles of colloidal silica in order to provide a wafer surface that is suitable for growing an epitaxial layer thereon; and
etching the wafer surface with ions prior to polishing.

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JUN 28 2006